We claim:

1. A method for fabricating a MOSFET, comprising:

forming a hard mask on a surface of a semiconductor;

etching a trench in the semiconductor through an opening in the hard mask;

forming a first insulating layer inside the trench;

introducing a gate material into the trench, wherein the first insulating layer is between the gate material and the semiconductor;

forming a body region and a source region in the semiconductor adjacent to the trench;

oxidizing the gate material to form a second insulating layer overlying a remaining portion of the gate material, wherein the hard mask limits oxidation to areas that the hard mask exposes;

removing the hard mask;

depositing a third insulating layer;

etching an opening in the third insulating layer to expose the source region; and

depositing a contact material in the opening in the third insulating layer to thereby form a contact plug making electrical contact to the source regions.

2. The method of claim 1, wherein the hard mask comprises a layer of silicon nitride.

3. The method of claim 1, wherein the gate material comprises polysilicon.

4. The method of claim 1, wherein the depositing the third layer comprises flowing a layer of glass over a surface the second insulating layer and the semiconductor.

5. The method of claim 4, wherein the glass comprises borophosphosilicate glass.

6. The method of claim 1, wherein depositing the contact material comprise depositing a metal layer at a pressure of about two atmospheric pressures.

7. The method of claim 6, wherein the metal layer comprises tungsten.

8. The method of claim 1, further comprising depositing a barrier layer on a surface of the semiconductor in the opening through the third insulating layer.

9. The method of claim 1, wherein removing the hard mask exposes the source region while the gate material remains protected by the second insulating layer.

10. A method of fabricating a MOSFET, comprising:

forming a trench in a surface of a semiconductor, the trench defining a mesa;

forming a first insulating layer along a wall of the trench;

forming a gate in the trench, the gate being insulated from the semiconductor by the first insulating layer;

forming a body region of a first conductivity type and a source region of a second conductivity type in the mesa;

forming a second insulating layer over the mesa;

etching an opening in the second insulating layer;

depositing a metal opening to form a first metal layer in electrical contact with the source region;

planarizing the first metal layer to form a plug, a surface of the plug being coplanar with a surface of the second insulating layer; and

depositing a second metal layer over the second insulating layer and the plug.

11. The method of claim 10, wherein forming a second insulating layer comprises forming a glass layer.

12. The method of claim 10, wherein depositing a first metal layer comprises depositing a metal from the group consisting of tungsten and copper.

13. The method of claim 10, wherein planarizing the first metal layer comprises chemical-mechanical polishing.

14. The method of claim 10, wherein planarizing the first metal layer comprises etching.

15. The method of claim 10, wherein forming the trench comprising:
forming a hard mask having an opening overlying; and
etching the semiconductor through the opening to form the trench.

16. The method of claim 15, wherein forming a gate in the trench comprises depositing polysilicon into the trench.

17. The method of claim 16, further comprising oxidizing the polysilicon layer to form a top oxide layer overlying a remaining portion of the polysilicon layer.

18. The method of claim 17, further comprising removing the hard mask after oxidizing the polysilicon layer and before forming the second insulating layer.

19. The method of claim 18, wherein removing the hard mask exposes the source region while the polysilicon in the trench remains protected by the top oxide layer.